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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/822,197	04/09/2004	Kuo-Chi Tu	252016-2430	2371

47390 7590 09/09/2005

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EXAMINER	
THOMAS, TONIAE M	
ART UNIT	**PAPER NUMBER**
2822	

DATE MAILED: 09/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/822,197	TU ET AL.	
	Examiner	Art Unit	
	Toniae M. Thomas	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *33-53* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *33* is/are allowed.

6)☒ Claim(s) *34-36,41,42 and 48* is/are rejected.

7)☒ Claim(s) *37-40,43-47 and 49-53* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *05/19/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This action is a first Office action on the merits of Application Serial No. 10/822,197, which is a divisional of Application Serial No. 10/411,347 filed 10 April 2003, now US 6,720,232.

2. The preliminary amendment filed on 09 April 2004 canceled claims 1-32. Accordingly, claims 33-53 are currently pending.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 34-36 are rejected under 35 U.S.C. 102(b) as being anticipated by Choi (US 6,072,210).

The Choi patent discloses a DRAM structure (see figs. 1-8 and accompanying text). The structure comprises the following elements as recited in claim 34: trenched capacitors in a trench 16 through an insulating layer 12,

13 in a memory area (see fig. 2 and col. 2, line 66 - col. 3, line 2),[1] wherein each of the trenched capacitors comprises a bottom electrode 17 lining an opening in the insulating layer (see fig. 3 and col. 3, lines 7-10), a capacitor dielectric layer 18 disposed on the bottom electrode (see fig. 3 and col. 3, lines 10-11), and a top electrode 20 disposed on the capacitor dielectric layer (see fig. 5 and col. 3, lines 28-32), wherein an opening remains in the top electrode within the trench (see fig. 5); and a conductive line 21 disposed on the top electrodes and filling inside the opening and the trench continuously (see figs. 6, 7 and col. 3, lines 47-52), wherein the conductive line is no higher vertically than said top electrode (see fig. 7).

The DRAM structure further comprises a bit line contact 15 in the memory area through the insulating layer 12, 13 to a bit line, as recited in claim 35 (see figs. 1, 7 and col. 2, lines 61-65), wherein the bit line contact is not vertically higher than the trenched capacitors, as recited in claim 36 (see fig. 7).[2]

5. Claims 41, 42, and 48 are rejected under 35 U.S.C. 102(e) as being anticipated by Chiang et al. (US 6,656,785 B2).

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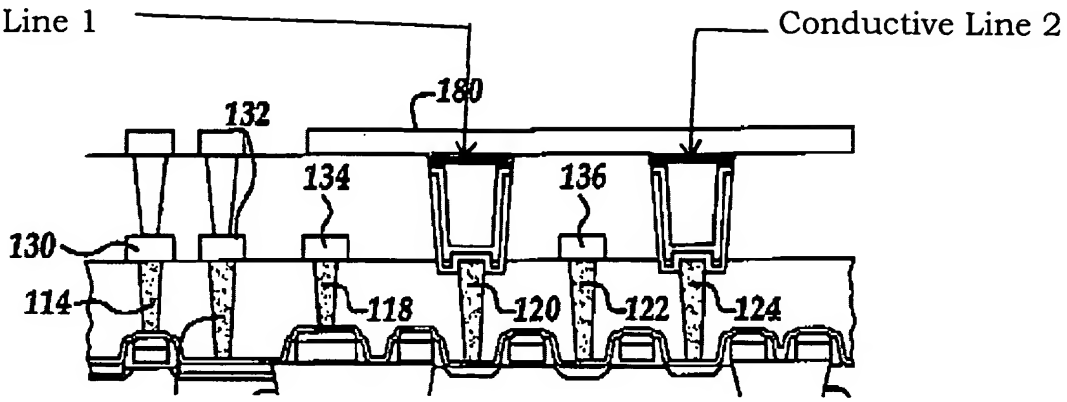
[1] The insulating layer 12, 13 is a laminate of insulating layer 12 and insulating layer 13.

[2] Typically, a DRAM memory cell comprises a capacitor and a bit line, wherein the capacitor is connected to one of two source/drain regions of a MOS transistor, and the bit line is connected to the other source/drain region. Often the capacitor and bit line are electrically connected to the source/drain regions via a capacitor contact and a bit line contact, respectively. Admittedly, Choi does not explicitly state that contact 15 in the DRAM memory cell is a bit line contact. However, since contact 14 serves as a capacitor contact between the capacitor and one source/drain region 3(4), it is inherent that contact 15 serves as a bit line contact between a bit line and the other source/drain region 4(3).

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

The Chiang et al. patent (Chiang) discloses an embedded DRAM and capacitor structure device (see figs. 11-18 and accompanying text). The device comprises the following elements, as recited in claims 41 and/or 48: trenched capacitors 150, 152 in two trenches through an insulating layer in a memory area of an integrated circuit (see fig. 17 and col. 8, line 46 - col. 9, line 8); a bit line contact 122 in the memory area through the insulating layer to a bit line wherein the bit line contact lies between the two trenches (see fig. 17 and col. 8, lines 35-36); and first line metal contacts 114, 116 in a logic area of the integrated circuit (fig. 17 and col. 8, lines 35-36), wherein the bit line contact and the first line metal contacts are not vertically higher than the trenched capacitors (see fig. 18). The structure further comprises two conductive lines 180 filling the two trenches respectively and continuously in contact with the trenched capacitors, as recited in claim 41 (see fig. 18 and col. 9, lines 18-22).[3]



Each trenched capacitor 150, 152 comprises a bottom electrode layer lining an opening in the insulating layer, a capacitor dielectric layer disposed on the bottom electrode, and a top electrode layer disposed on the capacitor dielectric layer, as recited in claim 42 (see fig. 16 and col. 8, line 51 - col. 9, line 8).

Allowable Subject Matter

6. Claim 33 is allowable over the prior art of record. The prior art of record does not anticipate, teach or suggest a embedded DRAM and capacitor structure device substantially as claimed, wherein the device comprises two twisted trenches.

7. Claims 37-40, 43-47, and 49-53 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Toniae M. Thomas whose telephone

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[3] The two conductive lines are those portions of metal layer 180 that fill the trenches above capacitors 150 and 152, respectively.

number is (571) 272-1846. The examiner can normally be reached on Monday through Friday from 8:30 a.m. to 5:30 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TMT
05 September 2005

AMIR ZARABIAN
EXAMINER
TECHNOLOGY CENTER 2800